WHAT IS CLAIMED IS:

1. An SRAM device, comprising:

a column of asymmetric memory cells spanning opposing bit lines in alternating orientations; and

a sense amplifier including:

sensing circuitry configured to sense stored values in said cells; and

switching circuitry configured to adapt the sensing circuitry as a function of said orientations.

2. The SRAM device as recited in Claim 1 wherein said column has only two of said opposing bit lines.

3. The SRAM device as recited in Claim 1 wherein said switching circuitry is configured to apply different voltage signals to opposing sides of said sensing circuitry.

4. The SRAM device as recited in Claim 1 wherein said orientations alternate based on a power of two.

5. The SRAM device as recited in Claim 1 wherein said orientations are based on threshold voltages of transistors in said cells.

6. The SRAM device as recited in Claim 1 wherein said switching circuitry receives a signal representing said orientations from a line of an address bus associated with said SRAM device.

7. The SRAM device as recited in Claim 1 wherein said asymmetric memory cells in said column are of a number that is a power of two.

8. The SRAM device as recited in Claim 1 wherein said orientations include first and second opposing orientations and said asymmetric memory cells are disposed equally in said first and second orientations.

9. An SRAM sense amplifier, comprising:

sensing circuitry configured to sense stored values in a column of asymmetric SRAM cells spanning opposing bit lines in alternating orientations; and

switching circuitry configured to apply voltage signals to said sensing circuitry as a function of said orientations.

10. The SRAM sense amplifier as recited in Claim 9 wherein said column has only two of said opposing bit lines.

11. The SRAM sense amplifier as recited in Claim 9 wherein said voltage signals comprise different voltage signals and said dummy bit line switching circuitry is configured to apply said different voltage signals to opposing sides of said sensing circuitry.

12. The SRAM sense amplifier as recited in Claim 9 wherein said orientations alternate based on a power of two.

13. The SRAM sense amplifier as recited in Claim 9 wherein said switching circuitry is configured to receive a signal representing said orientations from a line of an address bus associated with said SRAM cells.

14. A method of manufacturing an SRAM device, comprising:

providing opposing bit lines;

configuring a column of asymmetric memory cells to span said opposing bit lines in alternating orientations; and

coupling a sense amplifier to said opposing bit lines, including:

configuring sensing circuitry to sense stored values in said cells; and

configuring switching circuitry to apply signals to said sensing circuitry as a function of said orientations.

15. The method as recited in Claim 14 wherein said configuring said column includes configuring said cells to span only two of said opposing bit lines.

16. The method as recited in Claim 14 wherein said configuring said switching circuitry includes configuring said switching circuitry to apply different voltage signals to opposing sides of said sensing circuitry.

17. The method as recited in Claim 14 wherein configuring said column includes configuring said cell orientations to alternate based on a power of two.

18. The method as recited in Claim 14 wherein said configuring said cells includes configuring said cells based on threshold voltages of transistors in said cells.

19. The method as recited in Claim 14 wherein said configuring said sensing circuitry includes configuring said sensing circuitry to receive a signal representing said orientations from a line of an address bus associated with said cells.

20. The method as recited in Claim 14 wherein said configuring said cells includes configuring a number of said cells that is a power of two.

21. An SRAM device, comprising:

a first bit line;

a second bit line; and

a first SRAM cell having a first pass gate connected to said first bit line and a second pass gate wider than said first pass gate connected to said second bit line.

22. The SRAM device as recited in Claim 21 further comprising:

a second SRAM cell having a first pass gate connected to said second bit line and a second pass gate wider than said first pass gate connected to said first bit line;

a sense amplifier coupled to said first and second SRAM cells; and

switching circuitry coupled to said sense amplifier and configured to adapt said sense amplifier as a function of a selection of said first and second SRAM cells.